PLEASE ENTER TM 10/04/05.

IN THE CLAIMS

Please amend the claims as follows.

1-2. (Canceled)

3. (Previously Presented) A processor comprising:

a first memory configured to store a sequence of instructions representing essential code;

a second memory configured to store sequences of instructions representing non-essential code;

a conjugate mapping table configured with a plurality of triggers to specify respectively different sequences of the non-essential code to be executed from the second memory; and

a single microarchitecture structure configured to execute instructions both from the essential code and from the non-essential code, the processor being coupled to both the first and second memories to process code from the first memory, and to process code from the second memory in response to the triggers,

wherein the first memory is coupled to a first instruction cache configured to cache instructions that determine the logical correctness of a program,

wherein the second memory is coupled to a second instruction cache configured to cache instructions that provide hints for the execution of the instructions that determine the logical correctness of the program.

4. (Currently Amended) The processor of claim [[1]] 3 wherein the first memory is coupled to registers that store a microarchitectural state, and wherein the conjugate mapping table is responsive to the microarchitectural state.

5. (Currently Amended) The processor of claim ~~4 further comprising:~~

~~a first instruction cache coupled to the first memory;~~

[[a]] wherein the second instruction cache is coupled between the conjugate mapping table and the second memory.